| | Application No. | Applicant(s) |
|---|---|---|
| Notice of Allowability Exa | 10/791,172 | SPRINGER ET AL. |
| | Examiner | Art Unit |
| | Stanetta D. Isaac | 2812 |
| The MAILING DATE of this communication appe All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI | (OR REMAINS) CLOSED in to or other appropriate commun GHTS. This application is sub | his application. If not included ication will be mailed in due course. THIS |
| 1. A This communication is responsive to application filed on 03/01/04. | | |
| 2. 🔀 The allowed claim(s) is/are <u>10-13</u> . | | |
| 3. X The drawings filed on <u>01 March 2004</u> are accepted by the Examiner. | | |
| 4. | | |
| Attachment(s) 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/08 Paper No./Mail Date 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material | 6. ☐ Interview Sum Paper No./Ma), 7. ☐ Examiner's Am | il Date |

.

Application/Control Number: 10/791,172

Art-Unit: 2812

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 03/01/04. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

- 2. Claims 10-13 are allowed.
- 3. The following is an examiner's statement of reasons for allowance: Applicant's independent claim 10 is allowed over the prior art of record because none teach or render obvious an electronic system formed in a semiconductor layer, comprising, a channel stop implant region disposed in the semiconductor layer inwardly from portions of the field oxide layer and spaced apart from the periphery of the active region by an extension zone, the extension zone operable to inhibit the electrical interaction of the peripheral implanted regions of the transistor and the channel stop implant region. See Sato US Patent 5,242,849 where teaches an electronic system where channel stop implant regions are provided, however fail where the channel stop implant regions dispose inwardly from the portions of the field oxide layer and are spaced apart from the periphery of the active region by an extension zone.
- All dependent claims are also rendered allowable over the prior art of record. 4.
- 5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Application/Control Number: 10/791,172

Art-Unit:-2812

Page 3

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

- 7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
- 8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac Patent Examiner July 11, 2004

> Supervisory Patent Examiner Technology Center 2800)